OPTi Cache Sx/AT

Preliminary

82C281Data Book

Revision 1.1

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Patents Pending

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82C281/2 Design Specifications

Revision 1.0

September 5, 1991

1 82C281/2/82C282 Overview

The 82C281/2 is a highly integrated AT system logic VLSI for high end 386 Sx AT systems. It integrates the logic for local DRAM control, AT bus control, cache memory control, and data bus control and is designed for systems running at 16MHz, 20MHz, and 25MHz.

A high performance, compact 386 Sx/AT system can be implemented easily with 82C281/2 and standard peripheral controllers like the 82C206 or the VLSI 82C100 plus Dallas Semiconductor DS1287.

1.1 82C281/2 Features

1.1.1 Main Memory Subsystem

The 82C281/2 provides the following features in the memory subsystem:

A) Flexible DRAM Banks Configuration:

The 82C281/2 supports 256K, 1M, and 4M memory devices, total main memory size can be up to 16MB. A total of 12 different memory configurations are supported as shown in the following table..

Bank 0	Bank 1	Bank 2	Bank 3	Total
256K	256K	-	-	1M
256K	256K	256K	256K	2M
1M	-	-	-	2M
256K	256K	1M	-	3M
1M	1M	-	-	4M
256K	256K	1M	1M	5M
1M	1M	1M	-	6M
1M	1M	1M	1M	8M
256K	256K	4M	-	9M
1M	4M	-	-	10M
1M	1M	4M	-	12M
4M	4M	-	-	16M

b) Page Mode Operation:

Based on the memory configuration shown above, the memory control unit inside the 82C281/2 performs page mode of operation with a varying block size of 1k, 2k, or 4k bytes for 256k, 1M, or 4M DRAMs respectively.

c) System BIOS Shadow RAM:

The 82C281/2 memory control unit provides shadow RAM feature for several areas of memory - system BIOS, video BIOS, and adapter BIOS.

0F0000H - 0FFFFFH

The 0F0000H - 0FFFFFH system BIOS area can be programmed to:

Read with AT ROM cycle, write with local memory cycle (default).
Read with local DRAM memory cycle and write protected.

0C0000H - 0EFFFFH

The 0C0000H - 0EFFFFH area is divided into 12 16KB blocks and each block can be programmed to:

Read from AT bus, write to AT bus. (Default)
Read from AT bus, write to local DRAM.
Read from local DRAM, write to local DRAM.
Read from local DRAM, write protected.

d) Memory Remapping:

If shadow RAM feature is not utilized for the memory area between 0D0000H - 0EFFFFH, then memory remapping is possible . The local DRAM areas, 0A0000H - 0BFFFFH and 0D0000H - 0EFFFFH, a total of 256 KByte, are remapped to the top of total system memory. The areas for 0F0000H-0FFFFFH (system BIOS) and 0C0000H-0CFFFFH (Video BIOS) are reserved for shadow RAM purpose.

e) Flexible Multiplexed DRAM Address:

The following table describes how the DRAM address lines are multiplexed when different memory device types are used:

Address to MA Mapping

Mem	256K		1M		4M	
Addr	Col	Row	Col	Row	Col	Row
0	1	10	1	20	1	20
1	2	11	2	11	2	22
2	3	12	3	12	3	12
3	4	13	4	13	4	13
4	5	14	5	14	5	14
5	6	15	6	15	6	15
6	7	16	7	16	7	16
7	8	17	8	17	8	17
8	9	18	9	18	9	18
9			10	19	10	19
10					11	21

1.1.2 Cache Control Subsystem

Direct-mapped posted write cache control function provides a low cost alternative to enhance the system performance by up to 50%. In order to simplify the design without increasing the system cost or decreasing performance, the 82C281/2 has been designed to support only non-pipeline mode for systems with cache memory. The 82C281/2 offers the following cache control features:

1.1.2.1 Flexible Cache Memory Size

4MB Cacheable main memory by using 16KB low cost SRAM.
8MB Cacheable main memory by using 32KB low cost SRAM.
Cache 16MB main memory by using 64KB low cost SRAM.
Increase the cache size beyond 64KB up to 512KB

1.1.2.2 Cache Line Size 4 Byte

Burst mode memory prefetch is supported by the 82C281/2. During cache read miss cycles, the memory control subsystem will perform two consecutive read cycles to fetch 4 bytes from main memory before terminating the cycle by sending RDYO# signal to 386SX.

1.1.2.3 Non-Cacheable Area

The non-cacheable areas are predefined as indicated below:

I/O address space
memory address between 0A0000H and 0FFFFFH.
any memory address beyond the current configured memory size.
programmable non-cacheable memory area as defined by 82C281/2 internal registers.

1.1.2.4 82C281 Posted Write Cache

The 82C281 supports flexible direct-mapped cache with posted write through update of main memory. By programming the internal register, the post write control signals are provided by the 82C281 to support a one level write buffer. With posted write, the CPU write cycles can be completed in 2 CPU T-States, thereby increasing system performance.

1.1.2.5 82C282 Write Through Cache

The 82C282 supports a write-through cache system which allows the designer to reduce system cost by eliminating two F244's and two F373's with only a slight reduction in system performance (5-10%).

1.1.3 AT Bus Control

The 82C281/2 AT bus control unit handles all of the AT bus operations and the DMA/Refresh arbitration. The AT bus control unit supports the following features:

Programmable AT Bus Clock

The AT bus clock, ATCLK, can be programmed as CLK2/6, which is default, or CLK2/4.

Turbo Switch

The 82C281/2 provides a turbo switch feature that allows users to change the system clock speed. A programmable bit will enable or disable this turbo function. When the turbo function is enabled by setting reg[14H], bit[1] to 1, the 82C281/2 turbo pin then determines the system clock speed. A low on the turbo pin forces the cpu to run at the current AT bus speed which is CLK2/6 or CLK2/4.

2 System Operation

The following sections describe the detailed system operations of the 82C281/2 based Sx-AT design.

2.1 Reset

The power good (PWRGD) signal from power supply drives the system into the initial state when it is asserted low. The 82C281/2 forces CPURST, SYSRST, and NPRST high as soon as PWRGD becomes inactive. When the PWRGD is high, the chip de-activates the CPURST, SYSRST, and NPRST after 128 CLK2 cycles.

2.2 Cache Interface

The 82C281/2 cache control unit monitors the HIT# pin and the internal NCA# signals to determine if it is a cache hit or cache miss cycle. During the cache read miss cycle, the cache controller asserts TAGWE# to update the TAG RAM, CAWE# is also asserted to update the cache data memory.

The A1CNT output will be forced high then low to toggle CPU address bit 1 to cache data memory to achieve the prefetch.

During cache write hit cycles, the cache controller asserts the CAWE# signal to update the cache data memory.

2.3 Local DRAM Interfaces

Local DRAM is located on the CPU local data bus and is buffered by a F244 and F373 buffer. During CPU read cycles data is routed from main memory to CPU through F244's which are controled by LMRD#. During CPU write cycles, data is latched by F373 latches with the PDLTH signal from the 82C281/2 while DWE# controls the transceivers' enable. The main memory subsystem asserts the LMRD# while CPU, DMA, and external master card reads the local DRAM. DWE# is asserted during local DRAM memory write.

For local memory read cycles, the memory controller reads two bytes at a time. The read data passes into 82C281/2 where the parity checking function is executed.

For the local memory write cycles, the data bus control unit generates the parity bits to be stored into the local DRAM.

2.4 System BIOS ROM

If the system BIOS ROM is not shadowed, the ROM cycles are treated as AT cycles. The system designer can put the ROM on the XD bus as an 8-bit slave or SD bus as a16-bit slave.

For a 16-bit slave, ROMCS# is connected to M16# through an open collector driver such as a 7407, the 82C281/2 monitors M16# to determine the width of the ROM data path.

2.5 I/O Ports located on the XD bus

For I/O ports located on the XD bus, the XDIR# is activated. I/O ports 0F0H - 0FFH are reserved for the coprocessor.

2.6 Refresh Cycles

The AT bus control unit arbitrates the hold request from 82C206 and the refresh request from 82C281/2 internal, then decides which is the next owner of the bus once the CPU relinquishes it. The refresh request generated internally by 82C281/2 can be programmed as every15.9 micro-seconds or every 95.5 micro-seconds for slow refresh DRAM. If the bus is granted for refresh cycles, the AT bus control unit asserts RFSH# and MEMRD# commands and also generates the refresh address.

2.7 DMA Cycles

The hold request from the 82C206 initiates DMA/Master transfers. The 82C281/2 performs the arbitration between HRQ and refresh request. After the CPU acknowledges by asserting HLDA, and DMA request wins the arbitration, the 82C281/2 sends HLDA1 to the 82C206 acknowledging

the request. The 82C206 then asserts DMA16# and activates ADS16# to start 16-bit DMA transfers, or asserts DMA8# and activates ADS8# to start 8-bit DMA transfers.

2.8 Register Description

There are seven bytes of configuration register in the 82C281/2. An indexing scheme is used to access all the registers. Port 22H is used as an indexing register and Port 24H is used as the data registers. Every access to port 24H must be preceded by a write to port 22H even if the same register data is being accessed again. All reserved bits are set to zero by default. The default value of each bit is specified. The default values for register 10H Bit 5-0 are defined by the strapping of the MA0-5 pins outside 82C281/2 chip.

Index 10H - DRAM Configuration Register

BIT	Description
7,6	82C281/2 revision number. 00 is the initial number These two bits are read only.
5	Local DRAM Read Cycle Wait State. 1=2 wait states, 0=1 wait state.
4	Local DRAM Write Cycle Wait State 1=2 wait states, 0=1 wait state
3-0	Local DRAM Memory Configuration. See table below

BIT								
3	2	1	0	Bank 0	Bank 1	Bank 2	Bank 3	Total
1	1	1	1	256K	256K	-	-	1M
0	0	0	1	256K	256K	256K	256K	2M
0	0	1	0	256K	256K	1M	-	3M
0	0	1	1	256K	256K	1M	1M	5M
0	1	0	0	256K	256K	4M	-	9M
0	1	0	1	1M	-	-	-	2M
0	1	1	0	1M	1M	-	-	4M
0	1	1	1	1M	1M	1M	-	6M
1	0	0	0	1M	1M	1M	1M	8M
1	0	0	1	1M	4M	-	-	10M
1	0	1	0	1M	1M	4M	-	12M
1	0	1	1	4M	4M	-	-	16M

Index 11H - Shadow RAM Control Register

BIT	FUNCTION	DEFAULT
0	Shadow RAM at C0000H-CFFFFHread/write status. 0 = read/write 1 = read only.(while shadow RAM is being loaded, this must be set to 0; after it is loaded shadow RAM is write-protected by setting this bit to 1)	0
1	Shadow RAM at D0000H-DFFFFHread/write status. 0 = read/write 1 = read only.(while shadow RAM is being loaded, this must be set to 0; after it is loaded shadow RAM is write-protected by setting this bit to 1)	0
2	Shadow RAM at E0000H-EFFFFH read/write status. 0 = read/write, 1 = read only.(while shadow RAM is being loaded, this must be set to 0; after it is loaded shadow RAM is write-protected by setting this bit to 1)	0
3	Shadow RAM Copy Enable Control for C0000H to EFFFFH 0 = Write to the AT Channel 1 = Write to local DRAM	0
4	ROM located at C0000H-CFFFFH 0 = *All* accesses are on the AT channel and shadow RAM is disabled. 1 = Shadow RAM is selectively enabled in 16KB blocks by CFG Reg 13h; other accesses are AT channel cycles	1
5	ROM located at D0000H-DFFFFH 0 = *All* accesses are on the AT channel and shadow RAM is disabled. 1 = Shadow RAM is selectively enabled in 16KB blocks by CFG Reg 12h; other accesses are AT channel cycles	1
6	Adaptor ROM located at E0000H-EFFFFH 0 = *All* accesses are to System Board ROM, shadow RAM is disabled 1 = Shadow RAM is selectively enables in 16KB blocks by CFG Reg 12h, other accesses are *AT channel cycles*	1
7	Shadow RAM enable for system BIOS ROMat F0000H-FFFFFH. 1 = Reads go to ROM and writes go to shadow RAM 0 = *Read Only* from Shadow RAM	1

Index 12H - Shadow RAM Control Register II

This register selectively enables shadow RAM in 16KB blocks from D0000H to EFFFFH. These controls in conjunction with the Shadow RAM Register (CFG Reg 11H), are used to implement selective shadowing for the full range of systems implementations.

BIT	FUNCTION	DEFAULT
0	Shadow RAM enable in D0000H- D3FFFH area. 0 = Disable, 1 = Enable.	0
1	Shadow RAM enable in D4000H- D7FFFH area.	0
2	Shadow RAM enable in D8000H- DBFFFH area.	0
3	Shadow RAM enable in DC000H-DFFFFH area.	0
4	Shadow RAM enable in E0000H- E3FFFH area.	0
5	Shadow RAM enable in E4000H- E7FFFH area	0
6	Shadow RAM enable in E8000H- EBFFFH area.	0
7	Shadow RAM enable in EC000H- EFFFFH area.	0

Index 13H - Shadow RAM Control Register III

BIT	FUNCTION	DEFAULT
3-0	Remap address for unused shadow ram. Remaps A0000H-BFFFFH and D0000H - EFFFFH if not used for shadowing. Bits 3 - 0 correspond to address 23 - 20. See table below.	0000
4	1 = Enable Shadow Ram: C0000h-C3FFFH	0
5	1 = Enable Shadow Ram: C4000h-C7FFFH	0
6	1 = Enable Shadow Ram: C8000h-CBFFFH	0
7	1 = Enable Shadow Ram: CC000h-CFFFFH	0

A23	A22	A21	A20	Remap Address
0	0	0	0	no mapping
0	0	0	1	1MB
0	0	1	0	2MB
0	0	1	1	3MB
0	1	0	0	4MB
0	1	0	1	5MB
0	1	1	0	6MB
0	1	1	1	7MB
1	0	0	0	8MB
1	0	0	1	9MB
1	0	1	0	10MB
1	0	1	1	11MB
1	1	0	0	12MB
1	1	0	1	13MB
1	1	1	0	14MB
1	1	1	1	15MB

Index 14H - Miscellaneous Control register

BIT	FUNCTION	DEFAULT
0	AT Clock Select - A 0 sets ATCLK2 = CPUCLK2 / 6 A 1 sets ATCLK2 = CPUCLK2 / 4.	0
1	Enable Turbo Switch Function - turn on this bit enables turbo switch function.	0
2	Enable Slow Refresh Mode - 82C281/2 refresh request is generated internally every 15.9 micro-seconds. Setting this bit to a 1 will cause a refresh request to occur every 95 5 micro-seconds.	0
3	Reserved.	
4	Fast Non-Maskable Interrupt request.	0
5	Master Byte Swap Enable.	0
6	Keyboard Reset Control - if active, a HLT instruction must be executed before the 82C281/2 generates a CPU RESET from Keyboard Reset.	0
7	Znith Mode Enable - Setting this bit to a 1 will turn on znith mode which allows F0000H - F0FFFH to be written while write protect is on.	0

Index 15H - Cache Control register

BIT	FUNCTION	DEFAULT
2 - 0	Non-Cacheable Address Size - 82C281/2 allows user to specify a range as non-cacheable region. These three bits determine the size of that region. See table below.	111
3	Reserved. Must be programmed to 0.	
4	Absolute Non-Cacheable - turning on this bit causes all accesses to be non-cacheable.	1
5	1 = Enable Posted Write **(82C281 Only)** 0 = Disable Posted Write	0
6	Reserved. Must be programmed to 0.	
7	Cache Enable - A 1 indicates cache is installed. A 0 indicates cache is not installed.	0

Bits 2 1 0	Block size
0 0 0	64K
0 0 1	128K
0 1 0	256K
0 1 1	512K
1 0 0	2M
1 0 1	4M
1 1 0	8M
1 1 1	Disable

Index 16H - Cache Control register

This register is used in conjunction with Index 15H register to define a non-cacheable block. The starting address for the Non-Cacheable Block *must* have the same granularity as the Block size. For example, if a 1MB non-cacheable block is selected, its starting address is a multiple of 1MB; consequently, only address bits are A20-A23 are significant, A16-A19 are don't care..

BIT	FUNCTION	DEFAULT
7-0	Valid starting address bits A16-A23 of non-cacheable memory block 1. See table below.	00H

Block Size	Valid Starting Address Bits							
	A23	A22	A21	A20	A19	A18	A17	A16
64K	V	V	V	V	V	V	V	V
128K	V	V	V	V	V	V	V	X
256K	V	V	V	V	V	V	X	X
512K	V	V	V	V	V	X	X	X
2M	V	V	V	X	X	X	X	X
4M	V	V	X	X	X	X	X	X
8M	V	X	X	X	X	X	X	X

X = Don't Care

V = Valid Bit

2.13 AT compatible registers

2.13.1 I/O Port 61 (Port B)

The 82C281/2 provides access to Port B, IO port address 61H, defined for the PC/AT as shown in Table 1.1.

Port B Bit	Read/Write	Function
7	R	PCK - System parity check
6	R	IOCHCK - IO channel check
5	R	OUT2 - Timer 2 out
4	R	REFDET - Refresh detect
3	R/W	ENAIOCK - Enable I/O channel check
2	R/W	ENBRAMPCK - Enable RAM parity check
1	R/W	SPKRDATA - Speaker data
0	R/W	TIM2GATESPK - Timer 2 gate (speaker)

At power-on time, the NMI is disabled. However, it can be enabled or disabled by writing to IO port 70H with data bit 7 equal to zero or one respectively. An NMI occurs when NMI is enabled, ENAIOCK/ENBRAMPCK is enabled and an IOCHCK or PCK occurs.

2.13.2 I/O Port 92 - System Control register

BIT	FUNCTION	DEFAULT
0	Fast CPU Reset - Alternate fast CPU reset.	0
1	Fast GATEA20 - Alternate fast GATEA20.	0
7-2	Reserved Must be programmed to 0	

2.14 82C281/2 Pin Description

2.14.1 Clocks

Type	Pin No	Name	Description
I	43	CLK2	CLK2 Input from Oscillator
B	22	PCLK2	CLK2 Output to 386sx and 387sx (Bidirectional Output is always enabled)
O	104	OSC12	1.19 MHz Output.
I	18	OSC	14.31818 MHz Oscillator Input.

2.14.2 CPU Control Signals and Busses

Type	Pin No	Name	Description
I	67-55	A23:11	CPU Address bits 23-11
B	54-45	A10:1	CPU Address Bits 10-1. Normally they are input signals from CPU. They are outputs during refresh cycles.
B	44	A0	CPU Address Bit 0, it is input during CPU cycles, and output for non-CPU cycles.
B	9-2 158-151	LD15:0	Local Data Bus to/from CPU.
B	150,149	MP1:0	Local DRAM Parity Bits.
I	32	RDYI#	Ready Input from CPU Ready.
O	24	CPURST	CPU Reset Signal.
O	23	NMI	Non-Maskable Interrupt.
I	15	W/R#	Write/Read is a bus cycle definition pin that distinguishes write cycles from read cycles.
I	14	D/C#	Data/Control is a bus cycle definition pin that distinguishes data cycles from control cycles.
I	13	M/IO#	Memory/IO is a bus cycle definition pin which distinguishes memory cycles from input/output cycles.
I	12	ADS#	Address Status from 386sx.
O	11	HOLD	Hold Request to 386sx.
I	10	HLDA	Hold Acknowledge from 386sx
B	17	BHE#	Byte High Enable from CPU. It is input during CPU cycles, and output during non-CPU cycles.

2.14.3 DRAM Interface

Type	Pin No	Name	Description
O	127-130	RAS#3:0	Local DRAM Row Address Strobe Signals.
O	131-138	CAS#7:0	Local DRAM Column Address Strobe Signals
O	126-123	MA9:6	Multiplexed Row and Column Address Bit 9-6.
B	119-114	MA5:0	Multiplexed Row and Column Address Bit 5-0. MA5:0 are used to setup memory configuration and DRAM wait state control during system reset period. They are inputs during reset.
B	103	RFSH#	Refresh Cycles Indication Signal.
O	139	DWE#	DRAM Write/Read Control Signal.
O	25	LMRD#	Local DRAM cycles indication.

2.14.4 AT Bus Signals

Type	Pin No	Name	Description
T	107	ALE	AT Bus Address Latch Eanble. It is tri-stated during master cycles
B	105	XA0	System Board Latched Address Bit 0. It is an output for CPU, refresh, or 16-bit DMA cycles, and an input for 8-bit DMA or master cycles.
O	102	ATCLK	AT System Clock, ATCLK = CLK2/6 (default), ATCLK can be set to CLK2/4 by programming the internal registers.
B	98	SBHE#	System Byte High Eanble to/from AT bus. It is an input pin during master cycles.
B	97	MEMRD#	Memory Read Command Signal.
B	96	MEMWR#	Memory Write Command Signal
B	95	IORD#	IO Read Command Signal.
B	94	IOWR#	IO Write Command Signal.
I	145	0WS#	Zero Wait State Signal from AT Channel.
I	143	CHRDY	I/O Channel Ready Signal from AT Channel.
I	34	IO16#	I/O Data Size 16 Indication from AT Channel
I	142	M16#	Memory Data Size 16 Indication from AT Channel.
I	141	CHCK#	Channel Check Signal from AT Channel.
B	71-78 82-89	SD15:0	System Data Bus which are connected to AT Data82-89 Bus directly.

2.14.5 DMA Signals

Type	Pin No	Name	Description
I	112	DMA8#	8-Bit DMA Transfer Indication.
I	111	DMA16#	16-Bit DMA Transfer Indication.
I	113	HRQ	Hold Request from IPC
O	110	HLDA1	Hold Acknowledge 1 indicates CPU HLDA is caused by HRQ, not by refresh request.

2.14.6 Miscellaneous

Type	Pin No	Name	Description
O	106	KBDCS#	IO Port 60 and 64 Address Decode. It is de-activated during DMA cycles.
I	148	TURBO	Turbo Switch Control. CPUCLK2 = ATCLK2 if TURBO pin is low when turbo switch function is enabled.
O	147	GATE2	Timer 2 Enable Signal.
O	146	SPKD	Speaker Output.
O	144	LMGCS#	Low 1M Memory Decode Signal. This signal is also activated during refresh cycles.
O	93	INTA#	Interrupt Acknowledge Cycles Indication
I	92	PWRGD#	Power Bad Indication.
I	91	KBDRST#	CPU Reset Request from Keyboard Controller.
O	90	SYSRST	System Reset Signal.
O	140	ROMCS#	BIOS ROM Output Enable Signal
I	70	GATEA20	System Address Bit 20 Control from Keyboard Controller.
B	39	GA20	Gated Address 20. It is an input from master card during master cycles. During CPU cycles, GA20 is gated by GATEA20 or FAST GATEA20, during DMA cycle, GA20 = A20
O	109	GTA20	A20 control signal which is controlled by GATEA20 or FAST GATEA20 control bit from I/O Port 92 Bit 1.
O	69	XDIR#	XD Bus to/from SD Bus Direction Control.
O	108	ASRTC	Address Strobe for Real Time Clock
I	68	OUT2	Timer 2 Output.

2.14.7 Cache Interface

Type	Pin No	Name	Description
O	37	CAWE#	Cache Write Enable Signal which is activated during cache read miss cycles and cache write hit cycles.
O	36	CAOE#	Cache Output Enable Signal.
O	35	TAGWE#	TAG RAM Write Enable Signal is used to update the TAG RAM.
I	33	HIT#	Cache Hit/Miss Indication.
O	38	A1CNT	SRAM Address Bit 1 Control, used to toggle address bit 1 for pre-fetch cycles during cache read miss cycles.
O	26	PDLTH	Cache Post Write Through Data Latch Signal. **(82C281 Only. This pin is NC for 82C282.)**

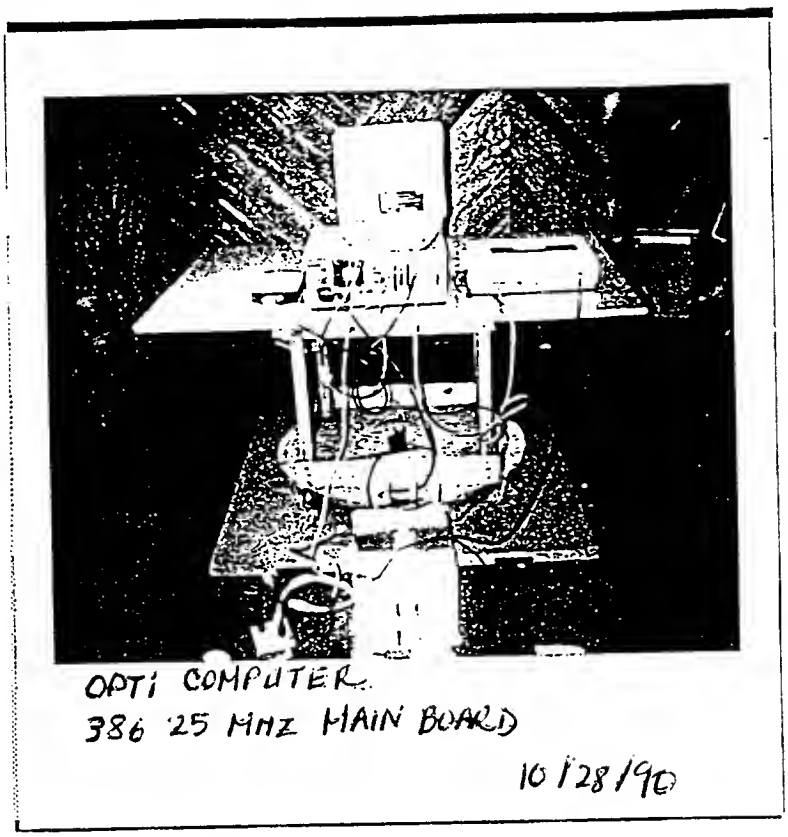
2.14.8 Numeric Processor

Pin No	Type	Name	Description
I	NPBUSY#	30	Numerical Coprocessor Busy Signal.
I	NPERR#	29	Numerical Coprocessor Error Signal.
O	NPRST	31	Numerical Coprocessor Reset
O	NPINT#	28	Interrupt Request 13 for 387sx Exception.
O	BUSY#	27	NP Busy and Error Status to CPU Busy Input.
O	RDYO#	16	Ready Output, ANDed with 387sx Ready# to generate RDYI#. RDYO# is not activated during Numerical Coprocessor cycles if 387sx is installed.

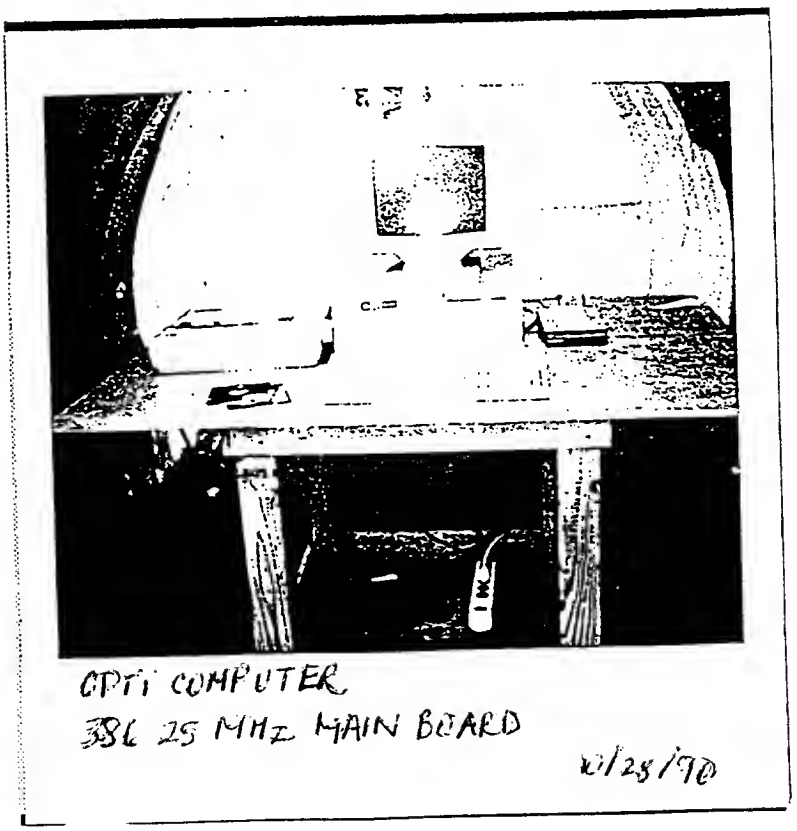
2.14.9 Power and Ground

Type	Pin No	Name	Description
I	1,20,40,81,100,120	Vcc	+5V
I	19,21,41,42,79,80,99,101,121,122,159,160	Vss	Ground

13.3 Test Configuration Photos



Line Conducted Test Setup



Radiated Open Field Test Setup

Compliance Engineering Services, Inc. P.O.BOx 612650 San Jose Ca 95161-2650 Tel:(408)463-0885 Fax:(408)463-0888

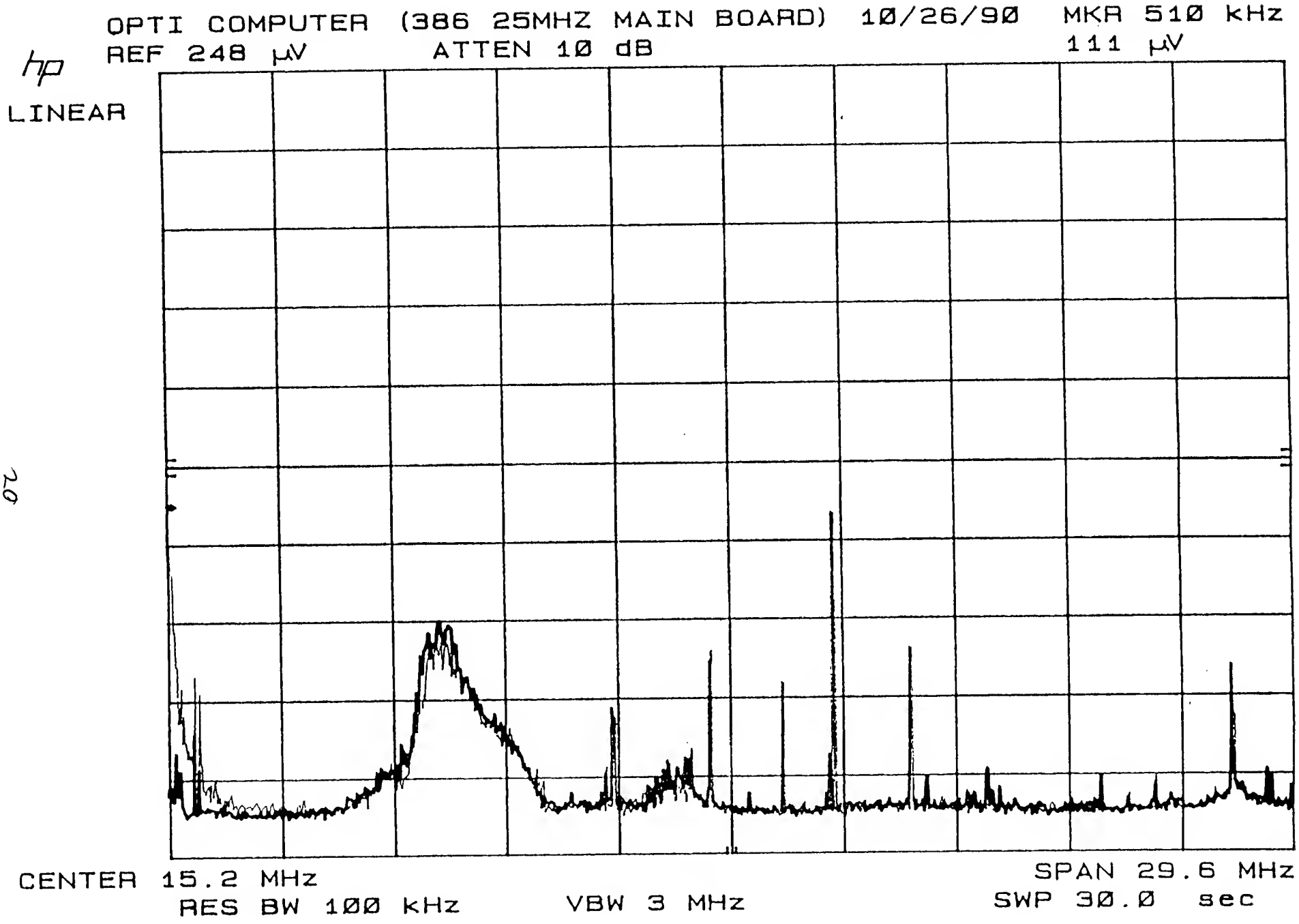
Compliance Engineering Services Inc.

Report No. : 901026A1
Date : 10/26/1990
Time : 11:34
Test Engr : TIM WANG

>> RADIATED EMISSION DATA <<

Company : OPTI COMPUTER
Equipment Under Test : 386 25 MHZ MOTHER BOARD
Test Configuration : EUT/NEC/EPSON/KB/DATATRONICS
Type of Test : FCC CLASS B
Mode of Operation : RUNNING AT 25 MHZ

Freq.	dBm	CF (dB)	dBuV	FCC-A	FCC-B	EUT-A	EUT-B	Note
40.36	-70.0	-13.2	23.8	49.5	40.0	-25.7	-16.2	Horizontal
44.04	-69.0	-12.9	25.1	49.5	40.0	-24.4	-14.9	Horizontal
50.00	-69.0	-12.5	25.5	49.5	40.0	-24.0	-14.5	Horizontal
58.00	-65.0	-15.2	26.7	49.5	40.0	-22.7	-13.2	Horizontal
69.31	-64.0	-16.9	26.1	49.5	40.0	-23.4	-13.9	Horizontal
75.00	-59.5	-14.3	33.2	49.5	40.0	-16.3	-6.8	Horizontal
100.00	-57.5	-14.2	35.2	54.0	43.5	-18.8	-8.2	Horizontal
107.27	-55.7	-14.4	36.9	54.0	43.5	-17.1	-6.6	Horizontal
121.08	-65.0	-12.8	29.2	54.0	43.5	-24.8	-14.3	Horizontal
125.00	-60.0	-11.4	35.6	54.0	43.5	-18.4	-7.9	Horizontal
133.34	-64.0	-8.2	34.8	54.0	43.5	-19.2	-8.7	Horizontal
141.67	-63.0	-5.1	38.9	54.0	43.5	-15.1	-4.6	Horizontal
150.00	-65.0	-5.1	36.9	54.0	43.5	-17.1	-6.6	Horizontal
166.68	-68.0	-3.8	35.2	54.0	43.5	-18.8	-8.3	Horizontal
175.00	-67.0	-5.1	34.9	54.0	43.5	-19.1	-8.6	Horizontal
177.10	-69.0	-5.9	32.1	54.0	43.5	-21.9	-11.4	Horizontal
178.83	-63.3	-6.6	37.1	54.0	43.5	-16.9	-6.4	Horizontal
179.19	-64.0	-6.7	36.3	54.0	43.5	-17.7	-7.2	Horizontal
225.00	-69.3	-10.1	27.6	57.0	46.0	-29.4	-18.4	Horizontal
250.00	-60.4	-8.2	38.4	57.0	46.0	-18.6	-7.6	Horizontal
275.00	-67.0	-6.7	33.3	57.0	46.0	-23.7	-12.7	Horizontal
300.00	-67.0	-3.5	36.5	57.0	46.0	-20.5	-9.5	Horizontal
450.00	-66.0	-0.4	40.6	57.0	46.0	-16.4	-5.4	Horizontal
500.00	-68.0	0.5	39.5	57.0	46.0	-17.5	-6.5	Horizontal
550.00	-71.0	4.2	40.2	57.0	46.0	-16.8	-5.8	Horizontal
575.00	-69.0	4.8	42.8	57.0	46.0	-14.2	-3.2	Horizontal
40.36	-65.0	-23.0	19.0	49.5	40.0	-30.5	-21.0	Vertical
44.02	-61.6	-22.3	23.1	49.5	40.0	-26.4	-16.9	Vertical
50.00	-62.4	-21.1	23.5	49.5	40.0	-26.0	-16.5	Vertical
58.34	-65.9	-19.8	21.3	49.5	40.0	-28.2	-18.7	Vertical
62.40	-66.0	-19.2	21.8	49.5	40.0	-27.7	-18.2	Vertical
66.06	-62.5	-18.7	25.8	49.5	40.0	-23.7	-14.2	Vertical
69.74	-60.7	-18.2	28.1	49.5	40.0	-21.4	-11.9	Vertical
75.00	-59.0	-17.6	30.4	49.5	40.0	-19.1	-9.6	Vertical
100.00	-55.1	-13.9	38.0	54.0	43.5	-16.0	-5.5	Vertical
107.27	-62.0	-13.3	31.7	54.0	43.5	-22.3	-11.8	Vertical
125.00	-58.9	-12.0	36.1	54.0	43.5	-17.9	-7.4	Vertical
151.79	-70.0	-9.6	27.4	54.0	43.5	-26.6	-16.1	Vertical
178.83	-66.9	-8.1	32.0	54.0	43.5	-22.0	-11.5	Vertical
250.00	-66.5	-8.2	32.3	57.0	46.0	-24.7	-13.7	Vertical
275.00	-70.0	-6.7	30.3	57.0	46.0	-26.7	-15.7	Vertical
350.00	-71.0	-4.4	31.6	57.0	46.0	-25.4	-14.4	Vertical
400.00	-64.4	-2.5	40.1	57.0	46.0	-16.9	-5.9	Vertical
450.00	-69.0	-0.4	37.6	57.0	46.0	-19.4	-8.4	Vertical
500.00	-67.8	0.5	39.7	57.0	46.0	-17.3	-6.3	Vertical


OPTI COMPUTER (386 25MHZ MAIN BOARD) 10/26/90
MKR 510 kHz
111 µV
REF 248 µV
ATTEN 10 dB
hp
LINEAR
CENTER 15.2 MHz
RES BW 100 kHz
VBW 3 MHz
SPAN 29.6 MHz
SWP 30.0 sec

1. VERIFICATION OF COMPLIANCE

Equipment Under Test:	80386SX 25MHZ MAIN BOARD
Model Number:	N/A
Serial Number:	N/A
Company:	OPTI,INC. 2700 AUGUSTISE DRIVE,SUITE#165 SANTA CLARA CA 95054
Type of Test:	CLASS B
Report Number:	90A0376
Date Tested:	OCTOBER 26,1990
Tested By:	TIM WANG
Result:	PASSED

The above equipment was tested by Compliance Engineering Services for compliance with the requirement set forth in the FCC Rules and Regulations Part 15, Subpart J. This said equipment in the configuration described in above report, shows the maximum emission levels emanating from equipment are within the compliance requirements.

STEVE CHANG / ENGINEER
OPTI,INC.

PAUL F. CHEN/SUPERVISOR
COMPLIANCE ENG. SERVICES,INC.
TESTING DIVISION

2. SCOPE

The Federal Communications Commission (FCC) establishes Rules and Regulations regarding the electromagnetic emissions of all electronic devices. An electromagnetic emissions test has been performed on the applicant/manufacturer's product to establish compliance with these Rules.

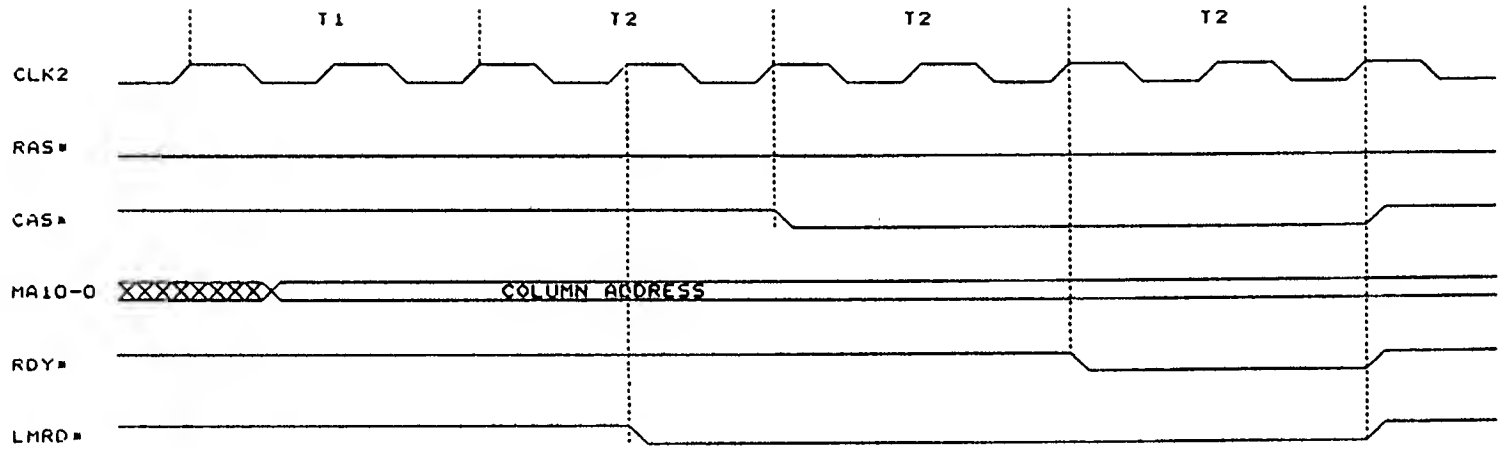
The test data contained in this report was obtained utilizing test procedures, equipment, and sites which were either approved by or prescribed by the FCC. The test procedures described herein are the established methods for the measurement of radio noise emitted from computing devices as defined in Section 15.4 of the FCC Rules. The technical standards for computing devices are set forth in Subpart J of Part 15 of FCC Rules (47 CFR 15-J). Methods for the measurement of radiated and powerline conducted radio noise are covered herein . These methods of measurement are those used by the FCC in testing computing systems, intended to be used with computing devices.

3. APPLICANT INFORMATION

Applicant:	OPTI,INC. 2700 AUGUSTISE DRIVE,SUITE#165 SANTA CLARA CA 95054
Contact Person:	STEVE CHANG / ENGINEER
Phone Number:	(408)980-8178
P.O. Number:	N/A
Product Tested:	80386SX 25MHZ MAIN BOARD
Model Number:	N/A
Serial Number:	N/A
Manufacturer:	OPTI ,INC. 2700 AUGUSTISE DRIVE SUITE 165 SANTA CLARA CA 95054
Type of Test:	CLASS B

4. PRODUCT INFORMATION

Product Description:	80386SX 25MHZ MAIN BOARD	
Housing Type:	METAL / BANDY,INC.	
Power Supply Type:	SWITCHING / SKYNET	
Line Filter Type:	BUILD IN POWER SUPPLY	
Line Cord Type:	SHIELDED	
Crystal Frequencies:	14.318 MHZ, 50MHZ.	
Memory:	1024 K	
Control Board:	WINCHESTER / WE1808530	
Floppy Drives:	TOSHIBA / BR118930	
Hard Drives:	NONE	
Keyboard:	SIIG / K101	ID: FK3459SKB101K
Monitor:	NEC JB-1406HMA	ID: A3D7Y6JB-1406HMA
Video Board:	EVEREX / EV-653	ID: E3E5UVEV653
Serial Board:	STB / SERPARAT	ID: EKS56ASERPARAT
Parallel Board:	STB / SERPARAT	ID: EKS56ASERPARAT
Host CPU:	EUT	
Other Equip.:	NONE	



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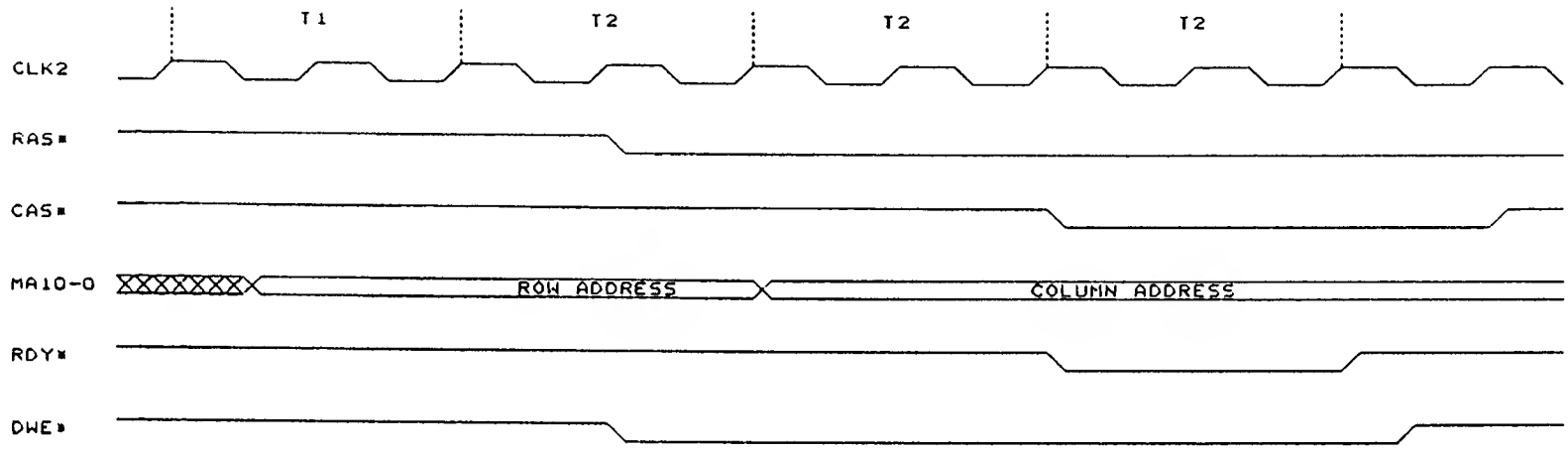
Date: September 24, 1990	Sheet	of



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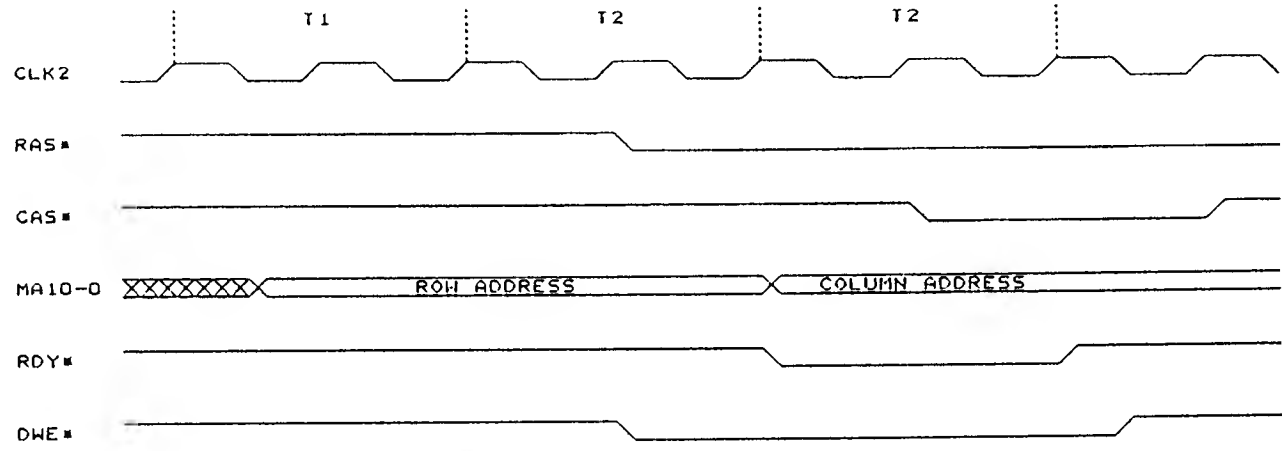

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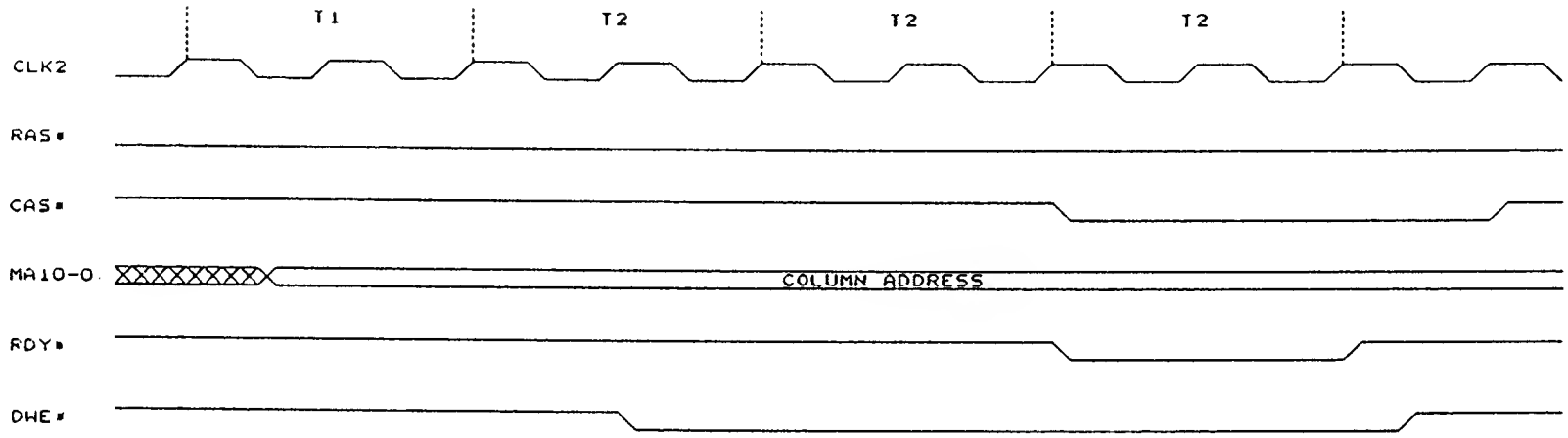

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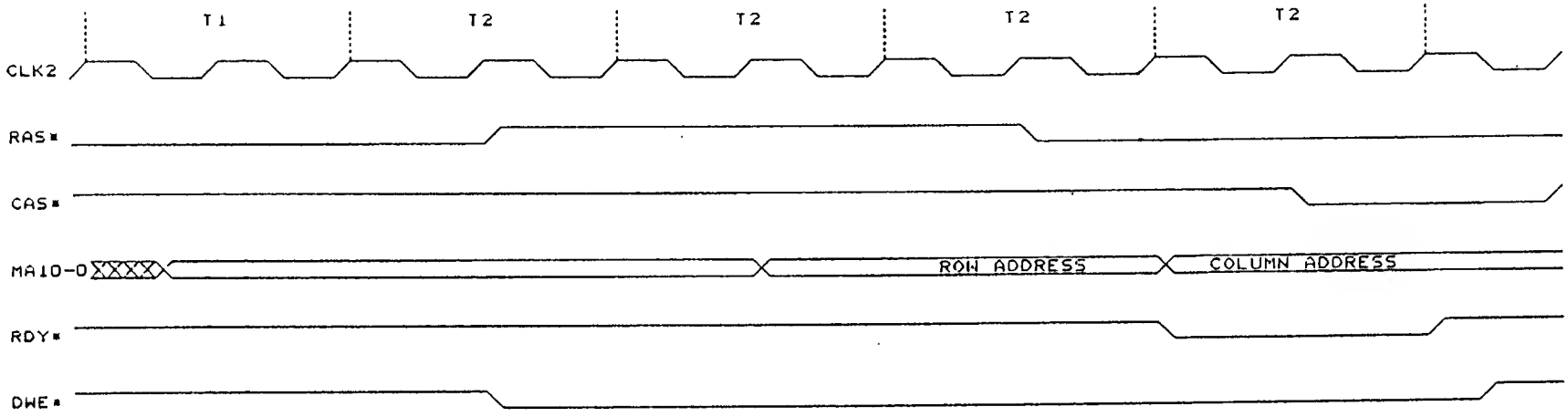

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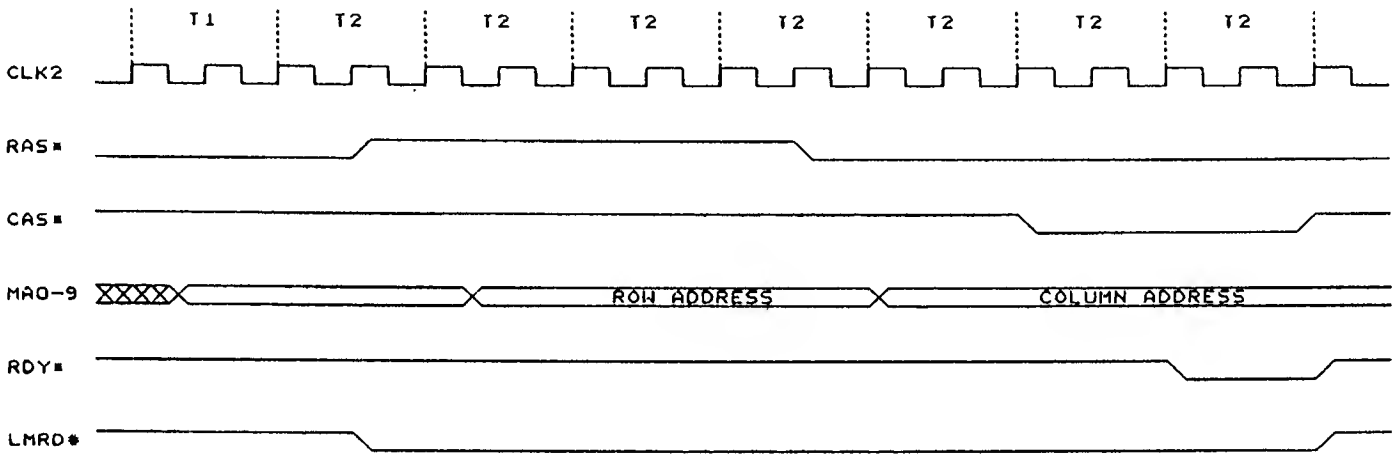

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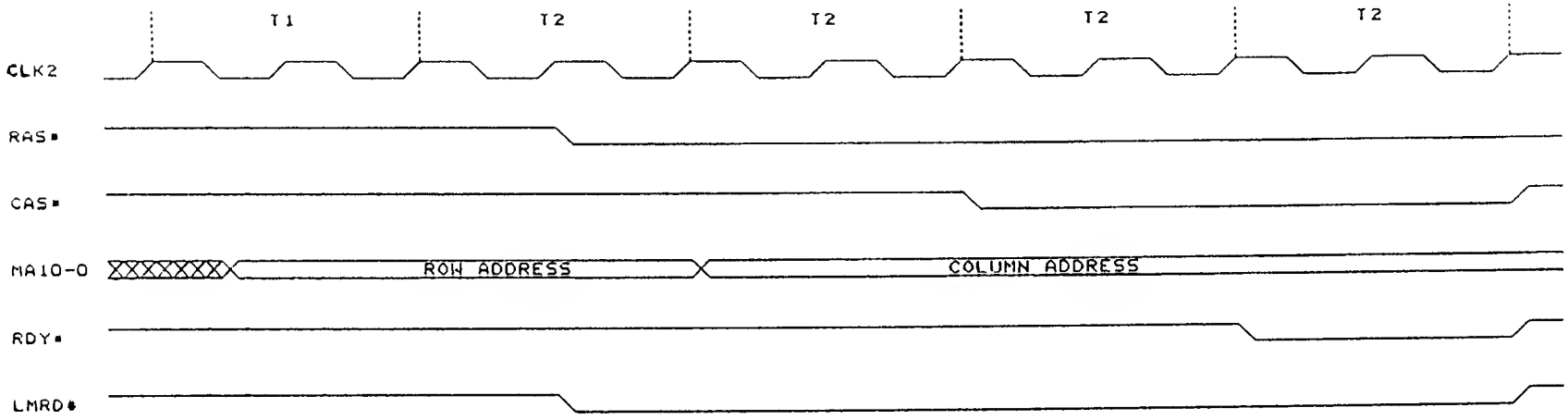

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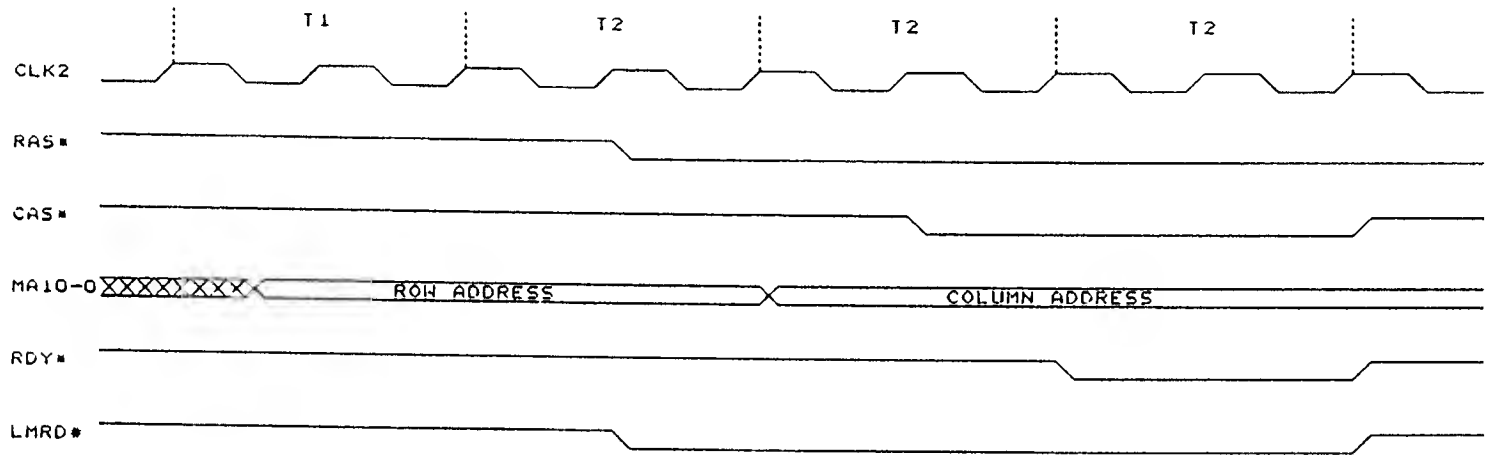

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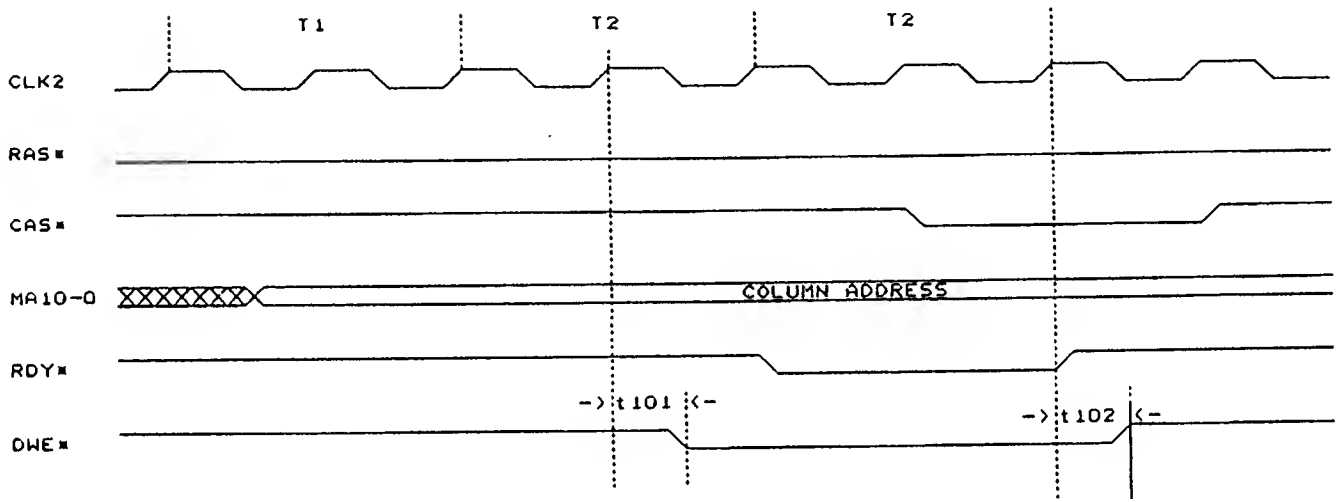

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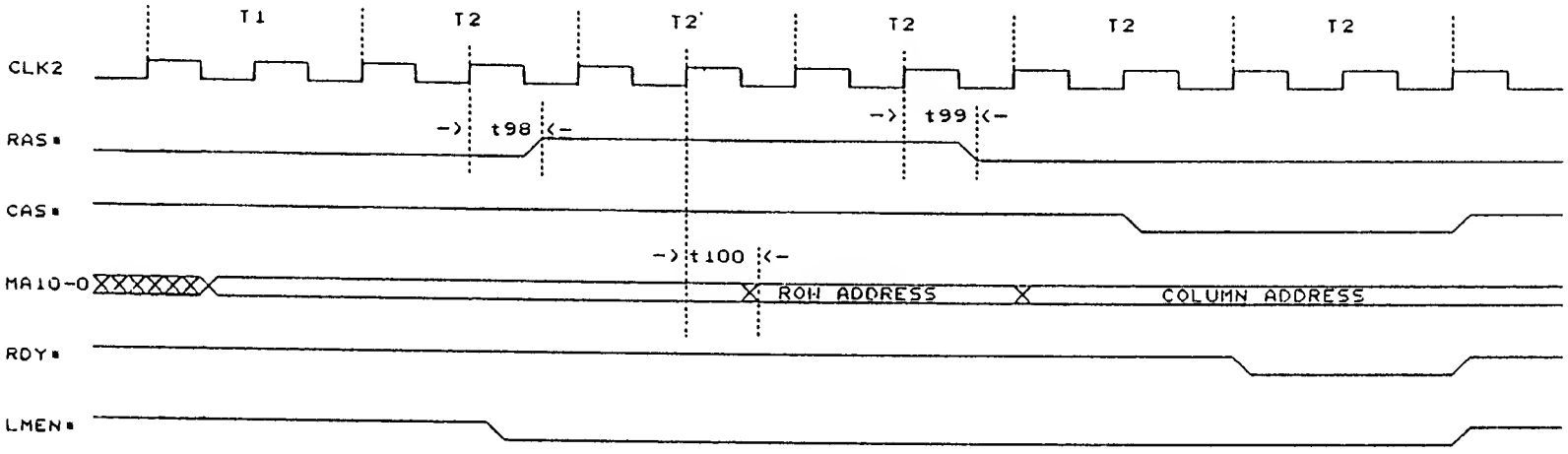

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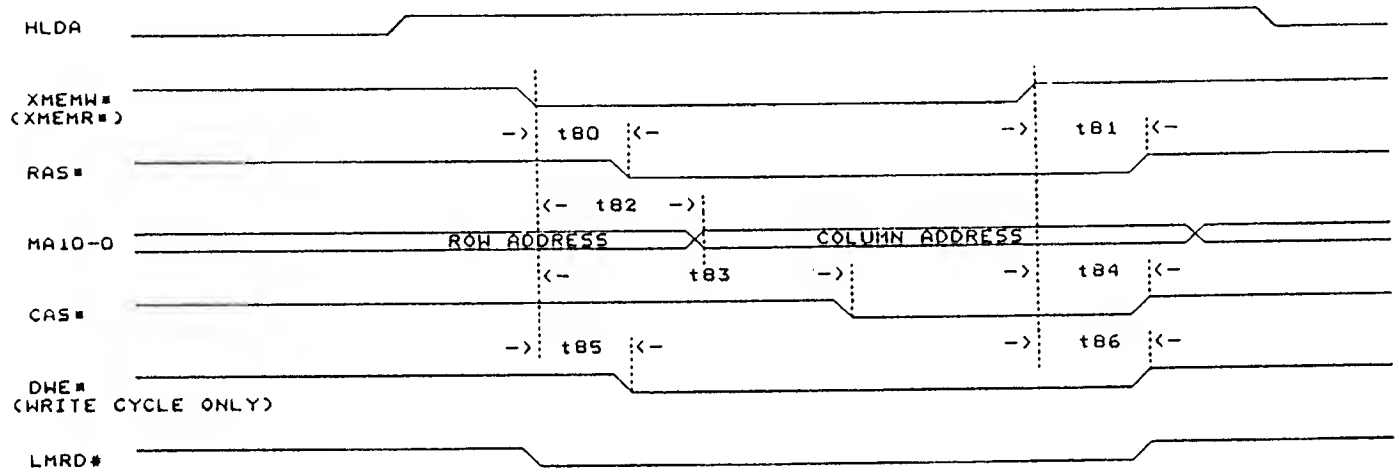

DMA/MASTER CYCLE

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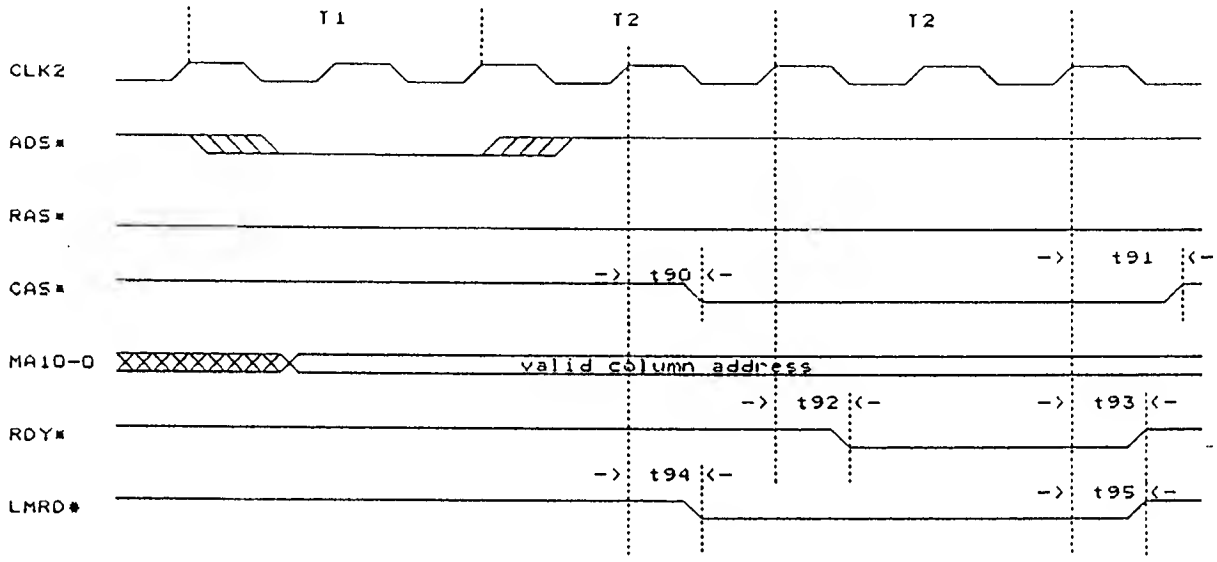

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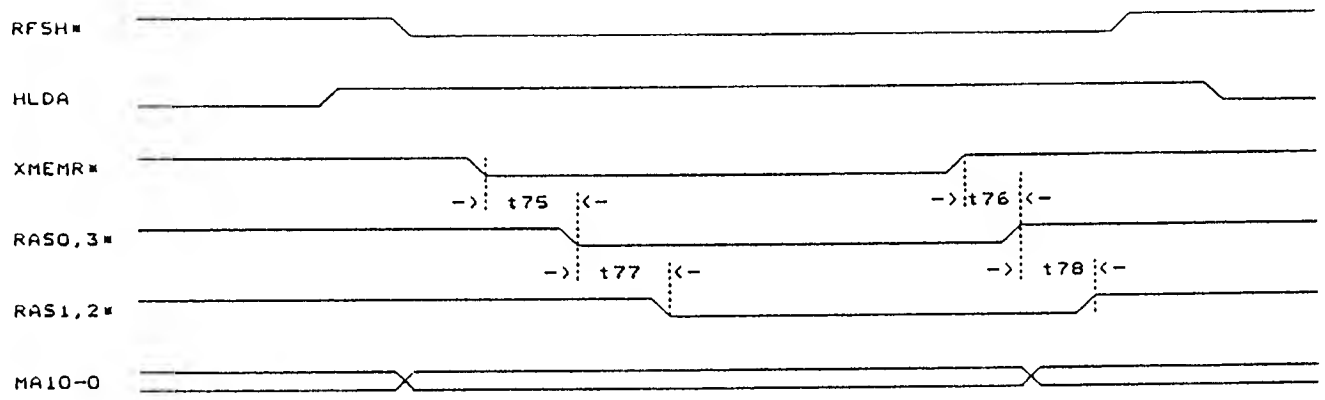

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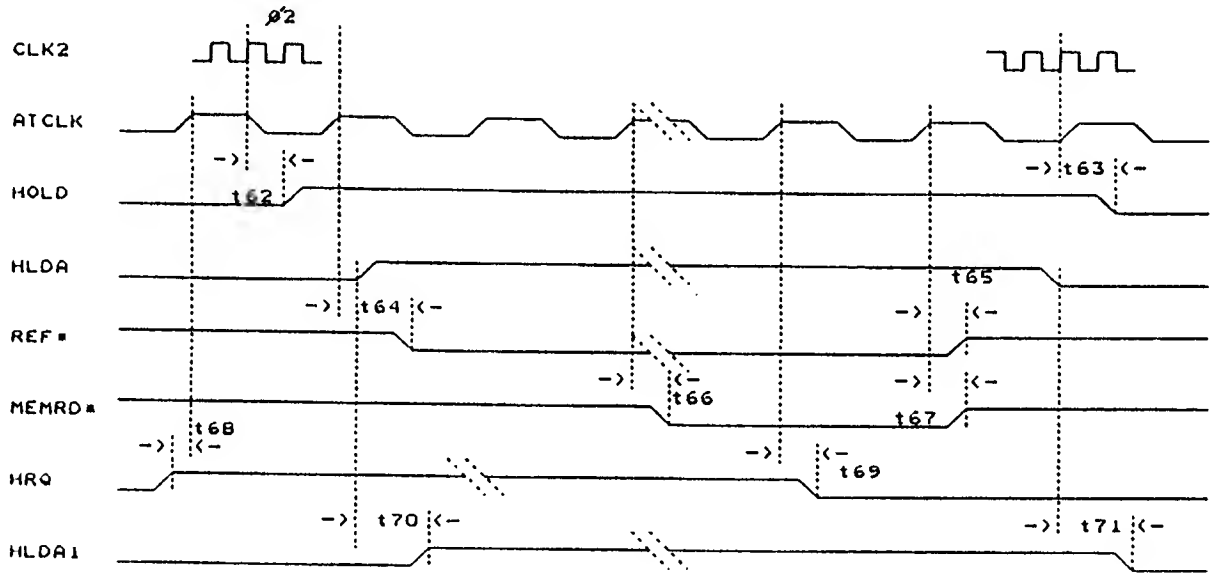

ATBUS HOLD TIMING

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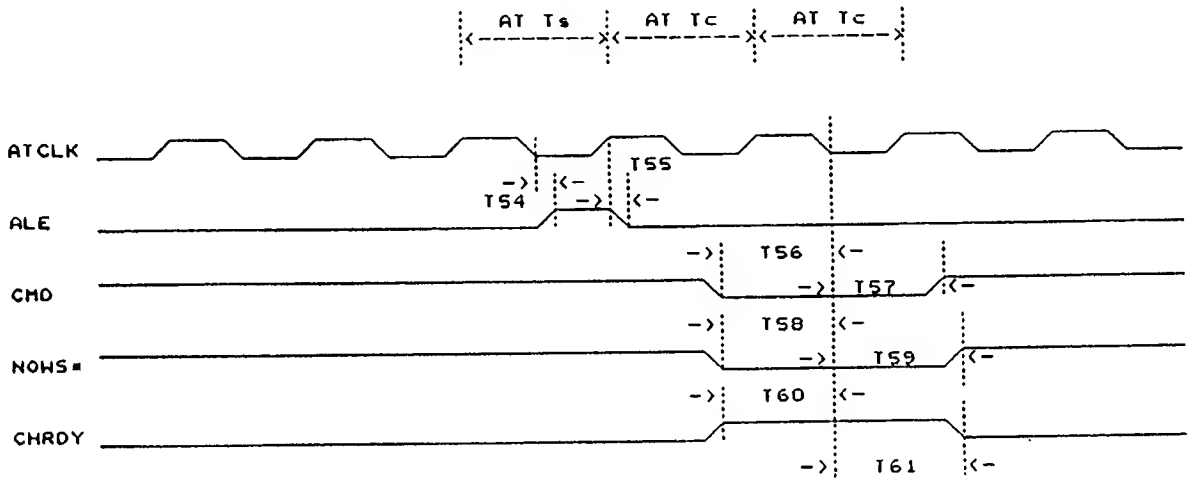

ATBUS TIMING

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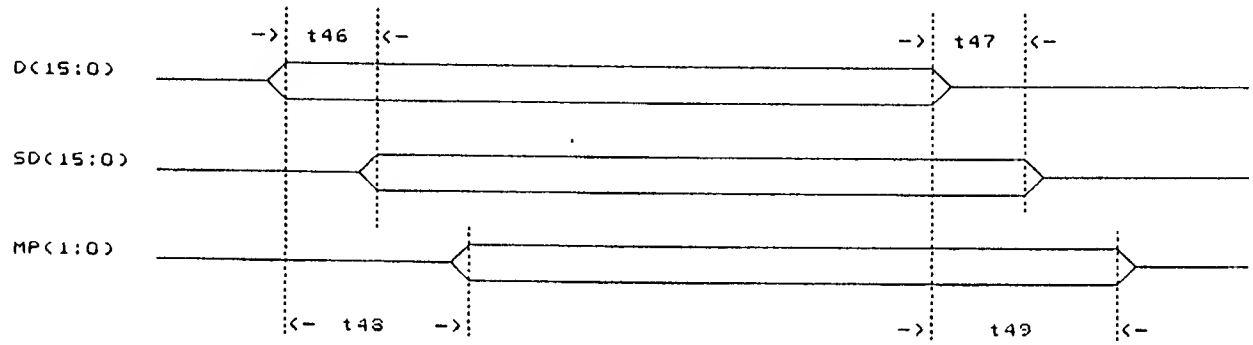
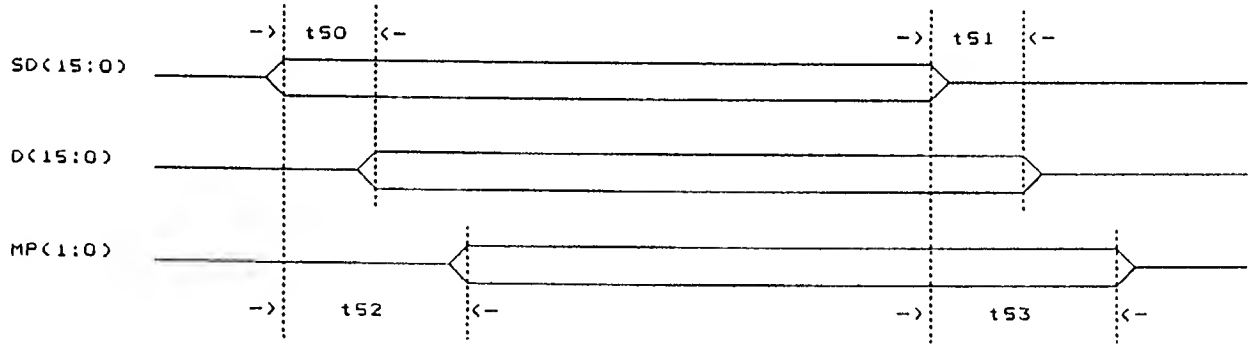


D(15:0) TO SD(15:0) & MP(1:0) VALID AND INVALID DELAY



SD(15:0) TO D(15:0) & MP(1:0) VALID AND INVALID DELAY

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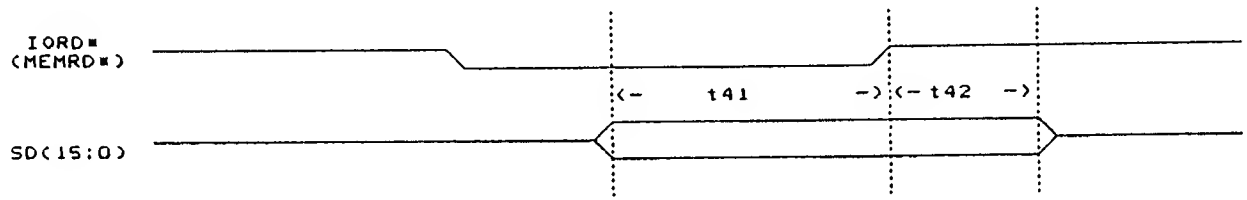
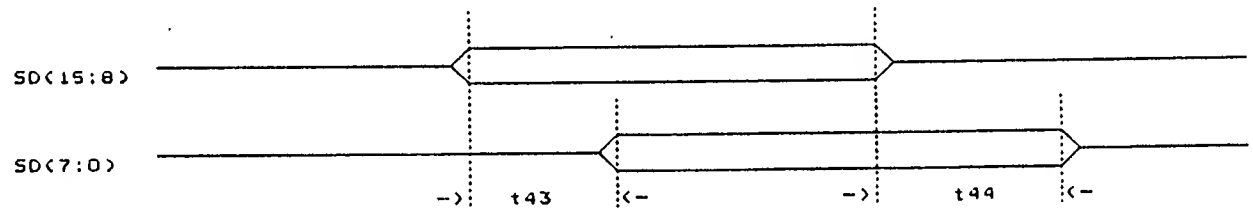
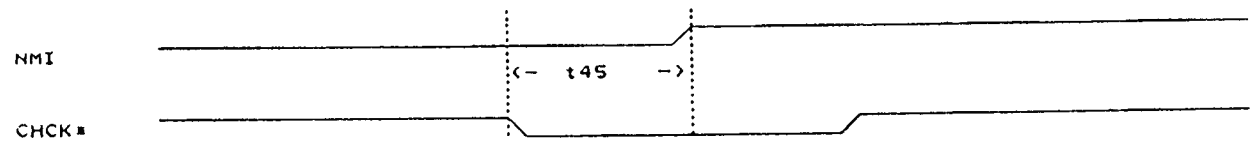
Date: October 7, 1990	Sheet of	



DATA SETUP AND HOLD TIME FOR IORD# OR MEMRD#



DATA VALID AND INVALID DELAY BETWEEN SD(15:8) AND SD(7:0) SWAPPING



NMI VALID DELAY RELATED TO CHCK#

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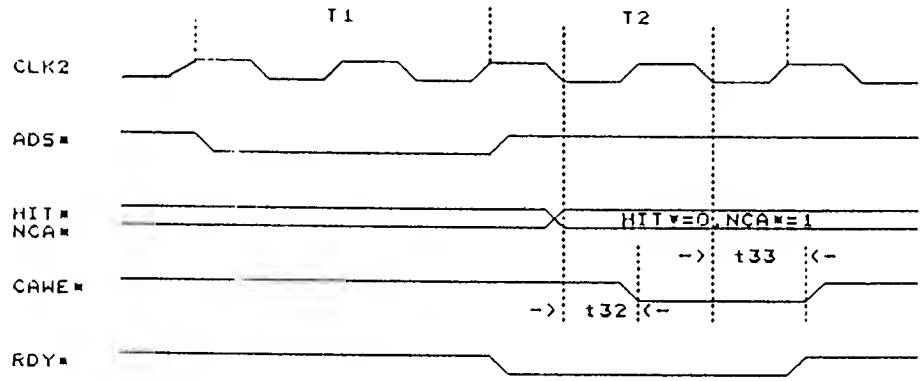

CACHE WRITE HIT CYCLE

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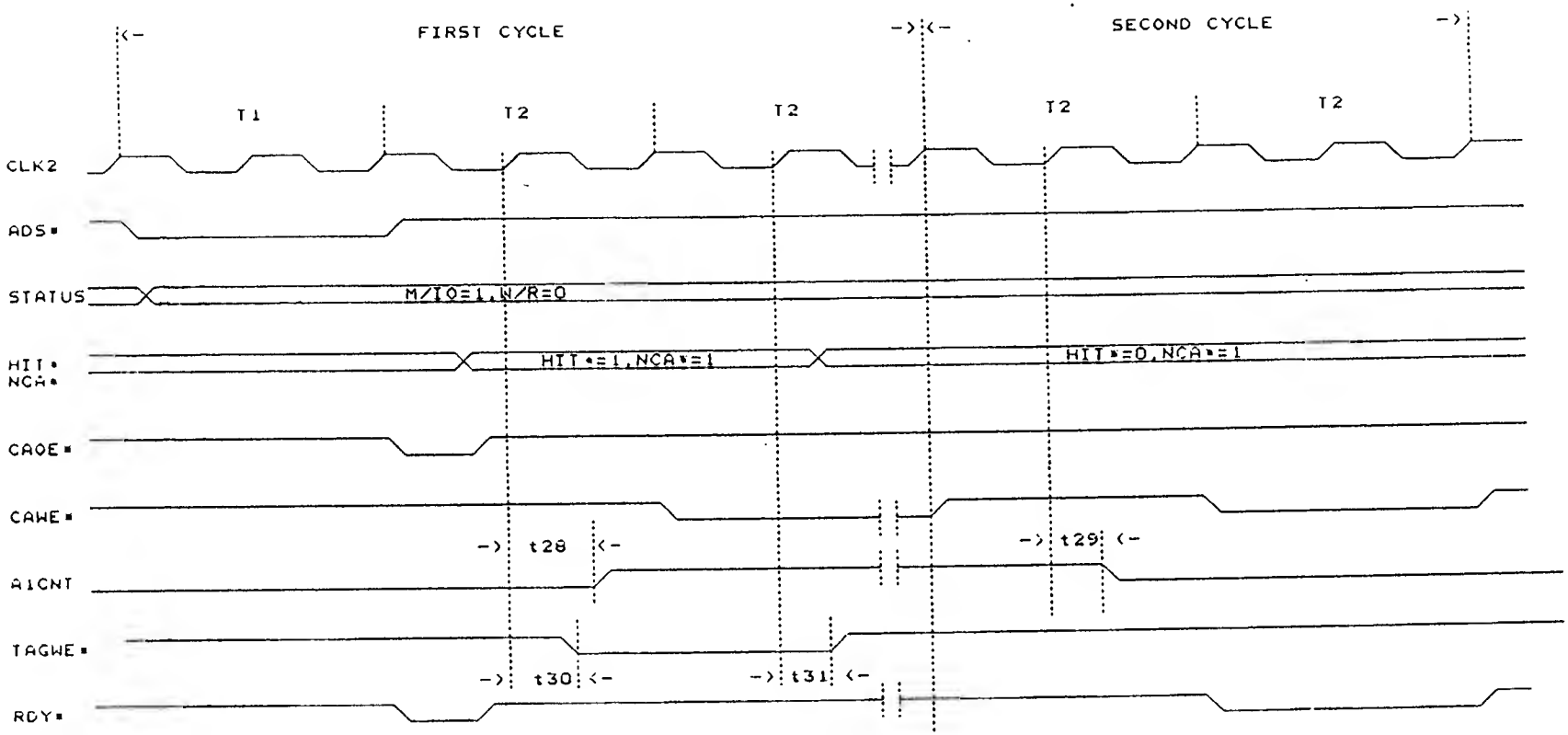

PREFETCH CYCLE (CACHE READ MISS)

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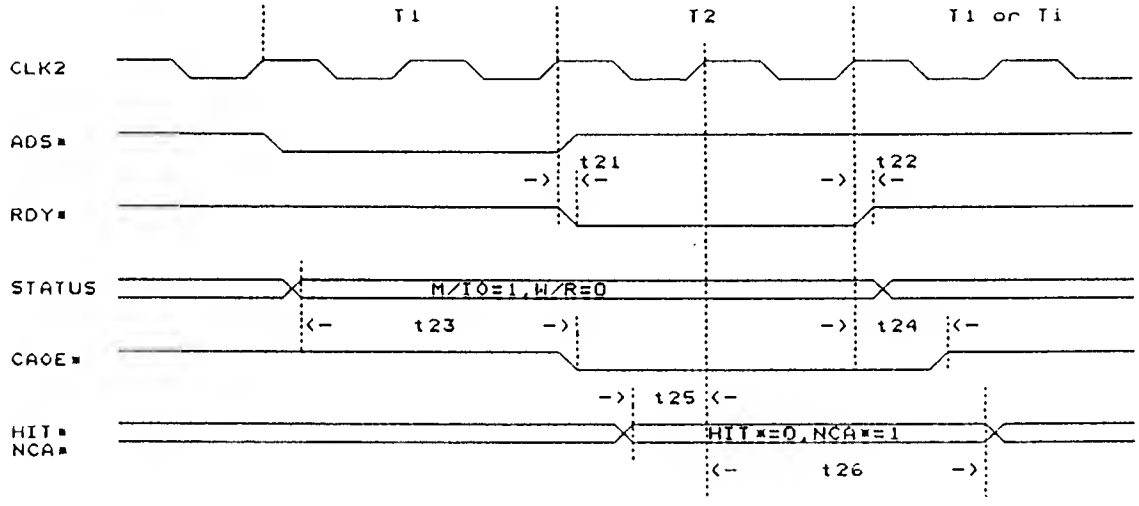

CACHE READ HIT CYCLE

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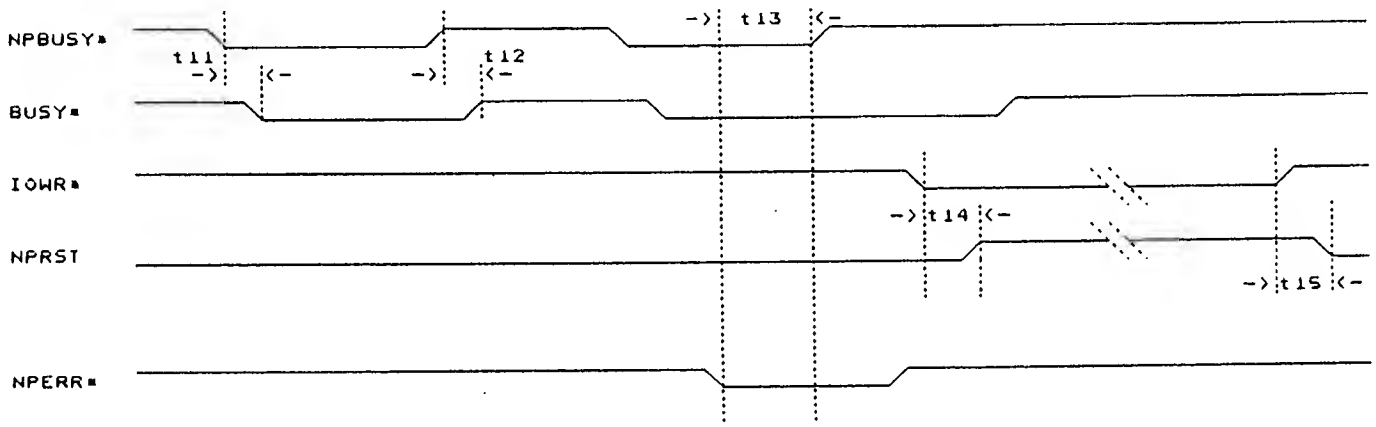

NUMERIC PROCESSOR RESET TIMING

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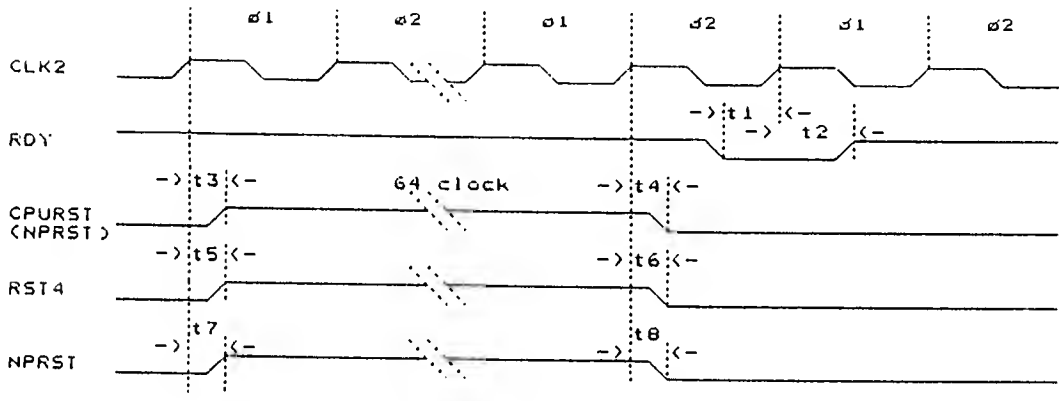

RESET TIMING

Size	Document Number	REV
A	OPTi-386SX	1
Date: September 20, 1990	Sheet of	

82C281/82C282-16/20 Mhz AC Characteristics
(TA = 0 C to 70 C, Vcc= 5V+/- 5%)

Sym	Description	Min	Max	Units
t1	Rdyi setup time to Clk2^	13		ns
t2	Rdyi hold time from Clk2^	3		ns
t3	Cpurst active delay from Clk2^	0	17	ns
t4	Cpurst inactive delay from Clk2^	5	12	ns
t5	Rst4 active delay from Clk2	0	17	ns
t6	Rst4 active delay from Clk2	0	17	ns
t7	Nprst active delay from Clk2	0	17	ns
t8	Nprst inactive delay from Clk2	5	12	ns
t11	Busy# active delay from Npbusy#		20	ns
t12	Busy# inactive delay from Npbusy#		20	ns
t13	Nperr# setup time to Npbusy#	5		ns
t14	Nprst active delay from low#		32	ns
t15	Nprst inactive delay from low# inactive		32	ns
t21	Rdy# active delay from Clk2^	4	20	ns
t22	Rdy# inactive delay from Clk2^	4	20	ns
t23	Caoe# active delay from status active		20	ns
t24	Caoe# inactive delay from Clk2^	5	25	ns
t25	Hit setup time to Clk2^	10		ns
t26	Hit hold time from Clk2^	10		ns
t28	A1cnt active delay from Clk2^		20	ns
t29	A1cnt inactive delay from Clk2^		20	ns
t30	Tagwe# active delay from Clk2^		20	ns
t31	Tagwe# inactive delay from Clk2^		20	ns
t32	Cawe# active delay from Clk2	13	19	ns
t33	Cawe# inactive delay from Clk2	9	14	ns
t41	Sd(15:0) setup time to lord#(Memrd#)	22		ns
t42	Sd(15:0) hold time from lord#(Memrd#)	3		ns
t43	Sd(15:8) active delay from Sd(7:0) valid	12	24	ns
t44	Sd(15:8) inactive delay from Sd(7:0) invalid	12	24	ns

82C281/82C282-16/20 Mhz AC Characteristics
(TA = 0 C to 70 C, Vcc= 5V+/- 5%)

Sym	Description	Min	Max	Units
t45	Nmi active delay from Chck# active		25	ns
t46	Sd (15:0) active delay from D(15:0) valid	10	25	ns
t47	Sd (15:0) inactive delay from D(15:0) invalid	10	25	ns
t48	MP (1:0) active delay from D(15:0) valid	10	27	ns
t49	MP (1:0) inactive delay from D(15:0) invalid	10	27	ns
t50	D (15:0) active delay from Sd(15:0) valid	10	25	ns
t51	D (15:0) inactive delay from Sd(15:0) invalid	10	25	ns
t52	D (15:0) active delay from Sd(15:0) valid	10	27	ns
t53	D (15:0) inactive delay from Sd(15:0) invalid	10	27	ns
t54	Ale active delay from Atclk^	0	15	ns
t55	Ale inactive delay from Atclk^	0	15	ns
t56	Command active delay from Atclk^	0	15	ns
t57	Command inactive delay from Atclk^	0	15	ns
t58	Nows# setup time to Atclk	15		ns
t59	Nows# hold time from Atclk	5		
t60	Chrdy setup time to Atclk	15		ns
t61	Chrdy hold time from Atclk	5		ns
t62	Hold active delay from Atclk	0	20	ns
t63	Hold inactive delay from Atclk	0	20	ns
t64	Ref# active delay from Atclk^	0	20	ns
t65	Ref# inactive delay from Atclk^	0	20	ns
t66	Memrd# atcive delay from Atclk^	0	20	ns
t67	Memrd# inative delay from Atclk^	0	22	ns
t68	Hrq setup time to Atclk^	15		ns
t69	Hrq hold time to Atclk^	20		ns
t70	Hlda1 active delay from hlda active	0	20	ns
t71	Hlda1 inactive delay from Hlda inactive	0	20	ns
t75	Ras(3:0)# active delay from Xmemr# active	0	20	ns
t76	Ras(3:0)# inative delay from Xmemrd# inactive	0	20	ns
t77	Ras(2 and 1)# active delay from Ras(3 and 0)	0	22	ns
t78	Ras(2 and 1)# inactive delay from Ras(3 and 0)	0	22	ns

82C281/82C282-16/20 Mhz AC Characteristics
(TA = 0 C to 70 C, Vcc= 5V+/- 5%)

Sym	Description	Min	Max	Units
t80	Ras# active delay from Xmemw#(Xmemr#)	0	22	ns
t81	Ras# Inactive delay from Xmemw#(Xmemr#)	0	22	ns
t82	Ma(10:0) active delay from Ras#	5	30	ns
t83	Cas# active delay from Xmemw#(Xmemr#)	20	40	ns
t84	Cas# inactive delay from Xmemw#(Xmemr#)	20	40	ns
t85	Dwe# active delay from Xmemw#(Xmemr#)	20	40	ns
t86	Dwe# inactive delay from Xmemw#(Xmemr#)	20	40	ns
t90	Cas# active delay from Clk2^	5	20	ns
t91	Cas# inactive delay from Clk2^	5	20	ns
t92	Rdy# active delay from Clk2^	4	20	ns
t93	Rdy# inactive delay from Clk2^	4	20	ns
t94	Lmrd# active delay from Clk2	5	20	ns
t95	Lmrd# inactive delay from Clk2	5	20	ns
t98	Ras# active delay from Clk2^	5	21	ns
t99	Ras# inactive delay from Clk2^	5	21	ns
t100	Ma(10:0) active delay from Clk2^	5	21	ns
t101	Dwe# active delay from Clk2^	5	20	ns
t102	Dwe# inactive delay from Clk2^	5	20	ns

Note:

1. Clk2^- Rising edge of Clk2
2. Clk2 - Falling edge of Clk2
3. Atclk^ - Rising edge of Atclk
4. Atclk - Falling edge of Atclk

82C281/82C282-16/20 Mhz DC Characteristics
(TA = 0 C to 70 C, Vcc= 5V+/- 5%)

Sym	Description	Min	Max	Units
VIL	Input low voltage		0.8	V
VIH	Input high voltage		2.0	V
VOL	Ouput low voltage IOL = 3.0 MA all pins except IOL = 6.0 MA for Group A IOL = 12.0 MA for Group B		0.4	V
VOH	Output high voltage IOH = -1.6 MA all pins except IOH = -3.2 MA for Group A IOH = -6.4 MA for Group B	2.4		V
IIL	Input leakage current, VIN=Vcc		10	UA
IOZ	Tristate leakage current		10	UA
CIN	Input capacitance		20	PF
COUT	Output capacitance		20	PF
ICC(20 Mhz)	Power supply current		50	MA

Group A pins : Ld(0:15), Mp (0:1), Rdyo#, Atclk, Ma(0:9), Ras(0:3)#, Cas(0:7)#

Group B pins : Ga20, Pclk2,Sd(0:15), Memrd#, Rfsh#, M16#

82C281/82C282 Absolute Maximum Ratings

Sym	Description	Min	Max	Units
VCC	Supply voltage		6.5	V
VI	Input voltage	-0.5	5.5	V
VO	Output voltage	-0.5	5.5	V
TOP	Operating Temperature	-25	70	C
TSTG	Storage temperature	-40	125	C

Note: Permanent device damage may occur if Absolute Maximum Ratings are exceeded.

USER'S GUIDE

DK/386SX-AT 1-chip Cache EVALUATION KIT

(Post-Write Cache)

September 7, 1990
Rev 1.0

OPTi, Inc., 2525 Walsh Avenue, Santa Clara, CA 95051 (408) 980-8178 FAX: 408-980-8860

OPTi

Table of Contents

A. Product Description

DK/SX-AT is a complete development kit for high performance 16/20/25 MHz Cache SX/AT systems. The evaluation board has the following features:

1. 16/20 MHz system operation
2. Upgradeable to 25 MHz operation
3. 16 MHz 386SX, socket for 387SX
4. 32KB of direct mapped Cache, upgradeable to 64K
5. 1 MB of memory on Memory Board, expandable to 16MB
6. 8 AT expansion slots
7. AMI/Microid SX/AT Evaluation BIOS ROM
8. 4-layer Baby AT form factor
9. Depending on whether you received the Post-Write or Write Thru TMP package, the diskettes with the following files:
    1. SX/AT Schematics in ORCAD 3.1
    2. Device Libraries
    3. BIOS HEX files from AMI, Microid, AWARD
    4. PADS-PCB layout database and Gerber Plots

B. Setup and Configuration

B.1 Basic Setup

To boot the DK/SX-AT, you need the following equipment:

1. AT compatible power supply
2. AT style keyboard
3. EGA card
4. EGA monitor
5. Floppy/Hard disk controller card
6. 5-1/4 high density floppy drive
7. Hard disk unit
8. Bootable DOS diskette
9. 1MB of 256K/1M or 4M SIMs

B.2 Using SETSX to change configuration registers

This document describes the usage of 82C281 SETSX.EXE utility and the procedure to boot up the OPTi 386SX Systems. Also it describes how to program 82C281 to get the best system performance.

Usage of 82C281 SETSX.EXE program:

Usage: SETSX [-c]

Functional Description:

The 82C281 SETSX.EXE program provides users a user friendly way to program the 82C281 chip.

In order to run SETSX, just type "SETSX" under DOS enviroment. It will display the current status of 82C281 on the screen. Use Up/Down arrow keys to move the cursor. The Left/Right arrow keys are used to change the content. After you have done the change, use ENTER key to program the 82C281 and save the Information into "SETSX.dat". If you decide to quit the SETSX without programming 82C281, use ESC key to exit the program.

The SETSX program will look for the data from "SETSX.dat" file if it exists in the current working directory. In order to force SETSX to read data from 82C281, you need "-c" option.

How to get the best system performance:

In order to get the maximum system performance, you should turn on BIOS Shadow RAM, also Video BIOS Shadow RAM on C4000H - C7FFFH and C0000H - C3FFFH areas. Set AT Bus Clock Freq. to CLK2 / 4. Turn on Slow Refresh Mode. Install the cache and turn on Post Write feature. And also turn off the Always-Noncacheable bit.

B.3 Upgrading the Evaluation Kit to 25 MHz

The DK/SX-AT can be upgraded from 20 MHz to 25 MHz. Even though Intel does not provide an SX rated at 25 MHz currently, OPTi has found that all 20MHz SX CPUs run at 25 MHz (and all C step 16MHz SX run at 20MHz). Consequently, by replacing the 16 MHz C-Step SX with a 20 MHz unit, the DK can be used to evaluate performance and compatibility at 25 MHz.

The changes that have to be made are:

- -Oscillator from 40 MHz to 50 MHz
- -CPU from SX-16 to SX-20
- -Tag SRAM from 25ns to 15ns
- -Cache SRAM from 35ns to 25ns
- -DRAM from 100ns to 80ns

D. Compatibility Test Report

OPTi has a compatibility testing program to ensure that OPTi products are compatible with industry standard hardware and software products, used by Personal Computer users.

OPTi's suite of hardware and software products includes products that are very popular, as well as products that are known to have compatibility sensitivities. Software products range from word processors, desktop publishing, spreadsheets, data base managers, benchmarks, utilities, operating systems to compute-intensive CAD software. Hardware products cover the spectrum from multi-function I/O, graphics, memory expansion cards, peripheral controllers to networking environments. In addition, OPTi alpha site OEMs provide intensive compatibility testing.

OPTi's goal is to provide its PC Compatible OEM's products a reputation for being on-par with COMPAQ in compatibility.

Testing Environment

The target SX-AT configuration is:

1. DK/SX-AT Evaluation Board, SX at 16/20/25 MHz
2. Direct Mapped 32 KB Cache
3. 16 MB of Main Memory
4. 1.2 MB 5-1/4" Floppy
5. 40 MB ST506 Hard Disk
6. Paradise 16-bit VGA
7. AT compatible generic Keyboard

Testing Methodology

The basic configuration of DK/SX-AT:

16MB of 80 ns DRAM SIMs
640KB of Conventional Memory, 15MB of Extended Memory
32 KB Cache enabled, post write
Video and System BIOS Shadowed

Software testing consists of configuring and installing the product, invoking and testing the various functions of the products.

Hardware testing consists of configuring and installing hardware on the target system; and exercising the hardware through diagnostic routines. For testing add-on memory boards, the Main Memory would be reduced appropriately.

The results are marked P (Pass), F (Fail), - (Not Applicable).

Results

All products tested were found to be compatible with the results produced by the reference system. See tables A and B for the detailed results.

Table A: Software Component Test Results

Type Software	Version	Results
Communication		
Crosstalk		P
Procomm		P
Data Base		
Paradox3		P
DBASE III	1.1	P
Framework II	1.1	P
Diagnostics/Demonstrations		
PC Labs Benchmark	4.2	P
Power Meter	1.2,1.5	P
Landmark	.99,1.12	P
QAPlus	3.01	P
Checkit		P
Coretest		P
IBM Advanced Diagnostics		P
Bus Master/DMA Diagnostics		P
Games/Educational		
Flight Simulator3		P
DugDigger		P
Word Processors		
Word	4.0	P
WordPerfect	4.2	P
Spreadsheets		
Lotus 123	2.01	P
Quattro		P
Symphony	2	P
Desktop Publishing		
PageMaker		P
Ventura with LIM 4.0	2.0	P
EMS Emulators		
QEMM		P

386MAX		P
LIM386		P
SEMMS		P

Operating Environments

IBM PC/DOS	3.3,4.0	P
IBM OS/2	1.1	P
SCO Xenix 386	2.3.2	P
Windows/286	2.11	P
Windows/386	2.11	P
Microsoft OS/2	1.10	P
DESQVIEW 386		P
Theos 386	3.0	P

CAD

Autocad	Rel9	P
ORCAD	1.2,3.2	P
Workview		P
MCAD		P
ORCAD-PCB Layout	1.2	P
ABEL		P

Utilities

Xtree	1.0	P
PCTools	4.24	P

Table B: Hardware Component Test Results

Type Hardware		Results
Communication		
Internal Modem		P
Hayes 2400B External Modem		P
Networking		
3COM 8/16-bit Ethernet Station		P
Novell Advanced Netware	2.12	P
- NE 2000		P
- Etherlink Plus 3C505		P
- Novell DCB Card	H	P
Novell Server		P
3COM 3+ Share/Etherlink Plus 3C505		P
Coprocessors		
80387sx		P
Controllers and Peripherals		
WD-1003 WA2(ST-506)		P
Seagate ST225 Hard Disk		P
Archive 2150L Tape Drive		P
ADAPTEC AHA-1540 SCSI (Master Card)		P
WD SCSI (Slave Card)		P
Cirrus Logic 1:1		P
NCL SCSI		P
DTC 5280i rev C +2 Controller		P
Display Monitors		
NEC		P
Sony		P
Input/Output Serial and Parallel Devices		
Mouse Systems Serial Mouse		P
Centronics Printer Port		P
Video Cards		
C&T EGA		P
Genoa EGA		P
Video 7 VGA Deluxe		P
Video 7 Fastwrite VGA		P

16-bit Paradise VGA	P
Orchid Designer 8-bit/16-bit	P
Matrox Graphics	P
Pixelworks	P
IBM VGA	P

Memory Cards

Intel Above Board	P
AST Rampage Card	P
BOCARAM	P
Everex 10000	P
JRAM-AT4	P

SEP 2 8 1992

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